

Required Course: **ECE421 –Advanced digital system design**

2005 Catalog Data: ECE 421: Advanced digital system design. Credit 3.
Advanced topics in digital design. Implementation of digital hardware systems based on the algorithms and implementation requirements using hardware description languages, optimization, logic synthesis, place and route methods. Special attention is given to the hardware programming using VHDL and Verilog as well as programmable design platform.

Prerequisites: ECE 266 or ECE 270. ENGR 197.

Prerequisites by Topic: 1. Digital circuits.
2. Computer programming.

Textbook: Charles H. Roth, Jr., *Digital Systems Design Using VHDL*, Second Ed., PWS Publishing, 2008 (ISBN: 0-534-38462-5)

References: Wayne Wolf, *FPGA-Based System Design*, Prentice Hall, 2004. ISBN: 0-13-142461-0.

Coordinator: Dr. Lauren Christopher, Assistant Professor of Electrical and Computer Engineering

Goals: FPGA-based digital design using VHDL or Verilog is a fundamental technique for many engineering applications. In this course, the students will study digital design, VHDL or Verilog, VLSI, and FPGA, and get exposure to the complete hardware design flow, Verilog/VHDL programming and hands-on experience in FPGA design and debugging.

Outcomes: Upon completion of the course, students should be able to

1. Understand complex digital design principles [b2, e]
2. Write synthesizable Verilog/VHDL programs [c, k]
3. Understand FPGA structure and usage [b2, e]
4. Know how to implement ASIC and FPGA design flow [b2, c, e]
5. Design, verify and test complex digital system in FPGA hardware [a, b2, c, e]

Topics: The course will cover the following topics.

1. Course Instructions, advanced topics in combinational and sequential logic (2 classes)
2. Advanced topics in logic for VHDL (3 classes)
3. VLSI design basics (2 classes)

4. PLD and FPGA structure (4 classes)
5. Verilog/VHDL basics (3 classes)
- 6.: Advanced Verilog/VHDL coding (7 classes)
7. FPGA design flow based on Verilog/VHDL (2 classes)
8. FPGA system implementation, verification and testing (3 classes)

Course Projects: The course will include five Homework, and five Lab Xilinx design projects, which involve programming using simulation and hands-on experiments. The students will submit short project reports for the first four small projects. Project 5 will be a term project requiring the students to submit a written project report and give a 10-minute presentation.

Lab 1: TBD

Lab 2: TBD

Lab 3: TBD

Lab 4: TBD

Project 5: Final Project – Student Selected

Computer usage:

The students are required to use Mentor Graphics Modelsim and Xilinx ISE software. They need to write their own Verilog/VHDL code for design projects.

ABET category: Engineering science 1.5 credits or 50%, Engineering design 1.5 credits or 50%.

Evaluation Method: **15% Five Textbook homework assignments,**
 20% Four design projects,
 25% Final Design Project,
 20% Midterm Exam
 20% Final Exam

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Updated: Lauren Christopher

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